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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,171	01/18/2002	Kenichi Watanabe	020029	7623

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,171	WATANABE, KENICHI	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *13 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-13,15 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-13,15 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE and Amendment filed on June 13, 2005.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-13, 15, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. (US 6,417,575 B2) in view of Lee et al. (US 6,163,074).

In re claims 9 and 15, Harada et al. shows (figs. 77A-77C) semiconductor device comprising a semiconductor substrate (1), a first interlayer insulating film (7) made of insulating material formed on the semiconductor substrate, and a first intra-layer insulating film (230) made of insulating material and formed on the first interlayer insulating film. The first intra-layer insulating film is formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part (lower wide portion of pad 240 in fig. 77B) and a wiring part (upper left extension of pad 240 within layer 230d) (or see left extension in fig. 77A), continuous with the pad part, the pad part having a width wider than a width of the wiring part. Insulating regions (341) are formed in the pad area. The pad seen in fig. 77A has a near wiring area superimposed upon an extended area of the wiring part into the pad part (imaginary near wiring area if wiring part extends partially into pad part to line 240). As seen in fig. 77A, a first frame area

has as an outer periphery (101) of the pad part and having a first width, and a second frame area has as an outer periphery an inner periphery (240) of the first frame area and having a second width. The device further comprises a first pad (material of 240) filled in the pad of the recess and a wiring filled in the wiring part of the recess. In another embodiment (figs.75A, 75B, 85A or 85B) upper surface of the first pad (portions of 240, 250, or 251), the wiring (portion of 240, 250, or 251) , and the insulating regions (301, 321, 331, 341) are on a same level. Harada shows all the limitations of the except the plurality of insulating regions (341) not disposed in a near wiring area superimposed upon an extended area of the wiring part into the pad part. As can be seen from the top view of fig. 77A, one insulating region (341) which is actually one continuous insulating layer surrounding the pad (240), is formed in a second frame area which has as an outer periphery an inner periphery of the first frame area. Instead, Lee et al. shows (fig. 9, 10, and 18) a semiconductor device having a pad portion (930) having a plurality of insulating regions (925 1) disposed on the bottom of the pad part. The insulating regions are disposed in a second frame area within a first frame area only. With this configuration (col. 2, lines 45-52) an improved contact pad is formed with reduced cracks. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the pad portion of Harada by forming a plurality of insulating regions on the bottom of the pad as taught by Lee to form an improved pad with reduced cracks.

In re claim 8, Harada shows (fig. 77C) a second interlayer insulating film (15) is formed on the first intra-layer insulating film, the first pad and the wiring. The second

interlayer insulating film is formed with at least one via hole (lower portion of 251), the via hole being superimposed upon the first pad. A second pad (101) is formed on the second interlayer insulating film and is connected to the first pad via a region in the via hole.

In re claim 10, Lee et al. shows (fig. 18) that the insulation regions (925 I or 945 I) are not disposed in a central area on an inner side of the second frame area.

In re claim 11, Harada shows (fig. 77A) in a top view that the via (251) is included in the first pad.

In re claim 12, Lee et al. shows (fig. 18) an alternate embodiment where a plurality of insulating regions (925 I or 945 I) are disposed regularly and have a first pitch (space between the insulating regions). As seen from the drawings, the width of the first frame area (width between lines of outer periphery of pad 960 and outer periphery of the first outside insulating region 945 I) is wider than the first pitch of the insulating regions.

In re claim 13, Lee et al. shows (fig. 10) that a wire bond step (990) is performed on the upper or second pad. The insulating regions (945 I) are not disposed in a central area on an inner side of the second frame area. In Harada (77A and 778) the via hole (251) of the upper or second pad is disposed in the central area. A contact area between the conductive wire and the second pad extends to an area on an outer side of the via hole as viewed from above because the wire bond would cover the top surface of the pad which has the via in its center.

In re claim 20, Harada shows (fig. 77B or 77C) that the bottom of the recess formed in the first intra-layer insulating film (230) is defined by the first interlayer insulating film (7).

Allowable Subject Matter

Claims 21-23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed with respect to claims 8-13, 15, and 20 have been fully considered but they are not persuasive. The applicant primarily asserts that the cited art does not show the amended limitation of the "upper surfaces of said pad, said wiring, and said insulating regions are on a same level." However, as stated in the rejection above other embodiments of the invention (particularly figs. 74B, 75B, and 85B). The insulating regions (301, 321, 331, and 341 in fig. 85B) have an upper surface that is same level as the upper surface of the pad (101) and the wiring part (300). Therefore, the cited references show all of elements of the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
mew
June 24, 2005

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER